

## APPENDIX B: THE MEMORY MAP

The following list describes where memory and peripheral devices are located in the addressing scheme of the Model 52. Devices include RAM and EEPROM memory as well as the I/O devices. The list begins at the top of the 64K memory space and proceeds down to zero.

Permanent EEPROM memory is not included.

FE00-FFFF, Not Used

FC00-FC0F, U8, 8256AH Multi-function Peripheral

- FC00 - Command Reg. 1 (DATA, STOP BITS)
- FC01 - Command Reg. 2 (PARITY, BAUD RATE)
- FC02 - Command Reg. 3 (INTERRUPT MODE)
- FC03 - Mode Register (COUNTER/TIMER CONFIG.)
- FC04 - Port1 Control Register
- FC05 - Interrupt Enable Register (EXT, COUNTERS, RS232)
- FC06 - Interrupt Address/Disable Register
- FC07 - Receive/Transmit Buffer
- FC08 - Port 1 (*CH A, CH B, CH Z* IN, *DIR* OUT)
- FC09 - Port 2 (*ISOLATED* OUTPUTS )
- FC0A - Timer 1 (not used)
- FC0B - Timer 2 (*CHA B* COUNTER (1) LOW BYTE)
- FC0C - Timer 3 (*STEP* COUNTER (2) LOW BYTE)
- FC0D - Timer 4 (*CH B* COUNTER (1) MSBYTE)
- FC0E - Timer 5 (*STEP* OUTPUT COUNTER (2) LOW BYTE)
- FC0F - Status Reg. (RECEIVER, TRANSMITTER STATUS)

FA00-FA0F, U9, 8256 Multi-function Peripheral

- FA00 - Command Reg. 1 (DATA, STOP BITS)
- FA01 - Command Reg. 2 (PARITY, BAUD RATE)
- FA02 - Command Reg. 3 (INTERRUPT MODE)
- FA03 - Mode Register (COUNTER/TIMER CONFIGURATION)
- FA04 - Port1 Control Register (7 in, 1 out)
- FA05 - Interrupt Enable Register
- FA06 - Interrupt Address/Disable Register
- FA07 - Receive/Transmit Buffer
- FA08 - Port 1 (QUADRATURE, *ISOLATED* INPUTS)
- FA09 - Port 2 (*PARALLEL* I/O CONTROL)
- FA0A - Timer 1
- FA0B - Timer 2 (+QUADRATURE COUNTER LOW BYTE)
- FA0C - Timer 3 (-QUADRATURE COUNTER LOW BYTE)
- FA0D - Timer 4 (+QUADRATURE COUNTER HIGH BYTE)
- FA0E - Timer 5 (-QUADRATURE COUNTER HIGH BYTE)
- FA0F - Status Reg. (RECEIVER, TRANSMITTER STATUS)

F800-F9FF, U16, 8255 *PARALLEL INPUT* Controller

- F803 - Control Register
- F802 - Port C Data Register (inputs 16-23)
- F801 - Port B Data Register (inputs 8-15)
- F800 - Port A Data Register (inputs 0-7)

F600-F603, U17, 8255 *PARALLEL OUTPUT* Controller

- F603 - Control Register
- F602 - Port C Data Register (outputs 16-23)
- F601 - Port B Data Register (outputs 8-15)
- F600 - Port A Data Register (outputs 0-7)

F400, - U26, AD7524 Digital to Analog converter

*ANALOG* Output Data Register

F200-F203, - U35, ADC0809 Analog to Digital converter

- F203 - ADC channel 3 - *IN 4*
- F202 - ADC channel 2 - *IN 3*
- F201 - ADC channel 1 - *IN 2*
- F200 - ADC channel 0 - *IN 1*

C000-EFFF, Not Used

A000-BFFF, U4, X2864 EEPROM

Non-volatile Read/Write Memory (8k X 8)

8000-9FFF, U3, X2864 EEPROM

Non-volatile Read/Write Memory (8k X 8)

location 8000H stores power up Baud rate and auto-run codes  
location 8010H stores the start-of-program character for the  
first stored program.

4000-5FFF, Not Used

2000-3FFF, U2, 6264 RAM

Read/Write Memory (8k X 8)

0-1FFF, U1, 6264 RAM

Read/Write Memory (8k X 8)

Use of RAM memory, from the top:

Top to MTOP: Model 52 receive buffers and operating variables

MTOP to VARTOP: declared program String space

VARTOP down: numerical program variables (6 bytes each)

DIMUSE up: dimensioned array variables

512 to DIMUSE: BASIC program, if any

0 to 512: BASIC operating variables and Argument Stack

(see MCS BASIC-52 USERS MANUAL Appendix 1.7)